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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/870,085	05/30/2001	Hiroyuki Yano	790001-2004	6781

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EXAMINER	
PHAM, THANHHA S	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 05/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/870,085	Applicant(s) YANO ET AL.	
	Examiner Thanhha Pham	Art Unit 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 23-48* is/are pending in the application.

4a) Of the above claim(s) *5,6,23-26 and 31-33* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,27-30 and 34-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action responses to Applicant's Amendment in Paper No. 16 dated 08/25/2003.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 3, 30, 36, 39, and 43 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

➢ With respect to claim 3,

lines 6-7, "following that a deep and irregular uneven portion is formed in the peripheral portion and the beveled portion of the target substrate" renders the claim indefinite. It is not clear which step following that a deep and irregular uneven portion is formed in the peripheral portion and the beveled portion of the target substrate -- selectively grinding or polishing the peripheral portion and the beveled portion **OR** forming at least a surface protecting film on the main surface of the target substrate.

➢ With respect to claim 30,

lines 13-15, "wherein the film remaining on the peripheral on the peripheral portion of the beveled portion is removed under a condition that the

film has non-selectivity to the semiconductor substrate" renders the claim indefinite. It is not clear that "the film" refers to which film of the process – the insulating film (as cited on line 3) **OR** the polysilicon film (as cited on line 7) **OR** both of the insulating film and the polysilicon film.

➢ With respect to claim 36,

lines 5-6, "following that a deep and irregular uneven portion is formed in the peripheral portion and the beveled portion of the target substrate" renders the claim indefinite. It is not clear which step following that a deep and irregular uneven portion is formed in the peripheral portion and the beveled portion of the target substrate -- selectively grinding or polishing the peripheral portion and the beveled portion **OR** forming at least a surface protecting film on the main surface of the target substrate.

➢ With respect to claim 39,

line 2-3, it is not clear how the anisotropic dry etching treatment is carried out so as to form a trench capacitor in the semiconductor. Suggestion: change "to form a trench capacitor in the semiconductor substrate " to "a trench in the semiconductor substrate" (see claim 40 for details)

➢ With respect to claim 43,

lines 5-6, "following that a deep and irregular uneven portion is formed in the peripheral portion and the beveled portion of the target substrate" renders the claim indefinite. It is not clear which step following that a deep and irregular uneven portion is formed in the peripheral portion and the beveled portion of the

target substrate – selectively grinding or polishing the peripheral portion and the beveled portion **OR** forming at least a surface protecting film on the main surface of the target substrate.

➢ With respect to claim 46,

line 2-3, it is not clear how the anisotropic dry etching treatment is carried out so as to form a trench capacitor in the semiconductor. Suggestion: change "to form a trench capacitor in the semiconductor substrate " to "a trench in the semiconductor substrate"

➢ With respect to claim 47,

it is not clear where "the trench" comes from and is located. Suggestion: change "the method of manufacturing a semiconductor device according to claim 44" to "the method of manufacturing a semiconductor device according to claim 46"

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 35-37 and 42-44 rejected under 35 U.S.C. 102(b) as being anticipated by Inaoka et al. [US 5,426,73] as submitted by IDS.

➢ With respect to claim 1, Inaoka et al. (figs 3's and col 1-8) discloses the claimed method of manufacturing a semiconductor device in which a semiconductor element is formed in the semiconductor substrate, including selectively grinding or polishing the peripheral portion and the beveled portion on the main surface side of a target substrate including a semiconductor substrate (1, figs 3a-3b,col 5 lines 13-17) wherein a film (multilayer 2) formed on the peripheral portion and the beveled portion is removed under a condition that the film has non-selectivity to the target substrate [see figs 3a-3b for details].

➢ With respect to claim 35, Inaoka et al. (figs 3's and col 1-8) discloses the claimed method of manufacturing a semiconductor device in which a semiconductor element is formed in the semiconductor substrate, including selectively grinding or polishing the peripheral portion and the beveled portion on the main surface side of a target substrate including a semiconductor substrate (1, figs 3a-3b,col 5 lines 13-17) wherein at least an uppermost layer (2-5) of multi-layered films (multilayer 2) formed on the peripheral portion and the beveled portion is removed under a condition that the at least uppermost layer (2-5) of the multi-layered films has non-selectivity to a layer (2-3) of the multilayer films which is under the at least uppermost layer of the muti-layered films [see figs 3a-3b for details].

➢ With respect to claim 42, Inaoka et al. (figs 3's and col 1-8) discloses the claimed method of manufacturing a semiconductor device in which a semiconductor element is formed in the semiconductor substrate, including selectively grinding or polishing the peripheral portion and the beveled portion on the main surface side of a target substrate

including a semiconductor substrate (1, figs 3a-3b,col 5 lines 13-17) wherein multi-layered films (multilayer 2) formed on the peripheral portion and the beveled portion is removed under a condition that the multi-layered films (2) has non-selectivity to the target substrate (1) [see figs 3a-3b for details].

➢ With respect to claim 2, Inaoka et al. (figs 3a-3b, see attachment) shows selectively grinding or polishing the peripheral portion and the beveled portion on the main surface side of the target substrate is carried out after a deep and irregular uneven portion is formed in the peripheral portion and the beveled portion of the target substrate.

➢ With respect to claims 4, 36 and 43, Inaoka et al. (figs 3a-3b, col 5 lines 1-28) discloses selectively grinding or polishing the peripheral portion and the beveled portion on the main surface side of the target substrate is carrier out after forming at least a surface protecting film on the main surface of the target substrate, said selectively grinding or polishing the peripheral portion and the beveled portion on the main surface side of a target substrate being carried out following that a deep irregular uneven portion is formed in the peripheral portion and the beveled portion on the target substrate.

➢ With respect to claims 5, 37 and 44, Inaoka et al. (figs 3a-3b, col 5 lines 1-28) discloses selectively grinding or polishing the peripheral portion and the beveled portion on the main surface side of the target substrate is carrier out after covering a portion (main surface where IC elements are formed) other than the peripheral portion and the bevel portion on the main surface of the target substrate, said selectively grinding or

polishing the peripheral portion and the beveled portion on the main surface side of a target substrate being carried out following that a deep irregular uneven portion is formed in the peripheral portion and the beveled portion on the target substrate.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 27-29, 38-40 and 45-47, as being best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Inaoka et al. [US 5,426,073] as in view of Jenq [US 5,795,804] and Nakayama et al. [US 6,291,315].

Inoaka et al. substantially discloses the claimed method but does not expressly teaches that selectively grinding or polishing the peripheral portion and the beveled portion on the main surface side of the target substrate is carried out after applying anisotropical dry etching treatment to form a deep and irregular uneven portion in the peripheral portion and the beveled portion of the target substrate *[claims 27, 38 and 45]* wherein the anisotropic dry etching treatment is carried out to form a trench in the semiconductor substrate and the trench is used for forming a trench capacitor formed on the semiconductor substrate.

However, Jenq (figs 1-12 and col 6 lines 6-42 and col 3 lines 10-42) teaches anisotropic dry etching to form a trench (5) in the semiconductor substrate wherein the

trench is used forming trench capacitor. Nakayama et al. (fig 13B, col 1-2) recognizes formation of deep and irregular uneven portion in the peripheral portion and the beveled portion of the target substrate when performing the anisotropic dry etch treatment to for the trench for trench capacitor.

Therefore, at the time of the invention, it would have been obvious for those skilled in the art to modify process of Inoaka et al. by performing anisotropic dry etch treatment to form the trench for trench capacitor as claimed as a demand of a semiconductor device being needed per taught by Jenq. It would also have been obvious for those skilled in the art, in view of Nakayama et al., to perform selectively grinding or polishing the peripheral portion and the bevel portion after the anisotropic dry etch treatment in the process of Inoaka et al. and Jenq to remove the deep and irregular uneven portion in the peripheral and beveled portion. By doing so, contamination caused by the deep and irregular uneven portions from the anisotropic dry etch treatment can be eliminated.

4. Claims 34, 41 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inaoka et al. [US 5,426,073] in view of Black et al. [US 6,265,314].

Inaoka et al. substantially discloses the claimed method including selective grinding or polishing the peripheral portion and the beveled portion of the target substrate. Inaoka et al. does not expressly teach selectively grinding or polishing the peripheral portion and the beveled portion while remaining a diameter of the semiconductor substrate substantially unchanged.

However, selectively grinding or polishing the peripheral portion and the beveled portion while maintaining the diameter of the semiconductor substrate substantially unchanged is a known technique to remove contaminant from the target substrate. See Black et al. as an evidence that shows selectively grinding or polishing the peripheral portion and the beveled portion while maintaining the diameter of the semiconductor substrate substantially unchanged.

Therefore, at the time of invention, it would have been obvious for those skilled in the art to modify process of Inaoka et al. by selectively grinding or polishing the peripheral portion and the beveled portion while maintaining the diameter of the semiconductor substrate substantially unchanged as a known technique as taught by Black et al to remove contaminant for the target substrate for making a better semiconductor device. By doing so, the target substrate is lessly damaged and a waste of substrate material can be reduced.

5. Claim 30, as being best understood, is rejected under 35 U.S.C. 103(a) as being unpatentable over Jenq [US 5,795,804] in view of Inaoka et al. [US 5,426,073].

Jenq (figs 1-12 and col 1-8) substantially discloses the claimed method of manufacturing a semiconductor device comprising steps of:

forming an insulating film (24, fig 1) on a main surface of a semiconductor substrate;

applying anisotropic etching to the insulating film and the semiconductor substrate so as to form a trench (5, fig 2, col 6 lines 6-21) in the semiconductor substrate; and

depositing a polysilicon (28, fig 3) on the main surface of the semiconductor substrate and in the trench.

Jenq does not teach after depositing the polysilicon film, selectively grinding and polishing the peripheral portion and a beveled portion on the main surface side of the semiconductor substrate wherein the insulating film and the polysilicon film remaining on the peripheral portion and the beveled portion is removed under a condition that the insulating film and the polysilicon film have non-selectivity to the semiconductor substrate.

However, Inaoka et al. teaches selectively grinding and polishing the peripheral portion and a beveled portion on the main surface side of the semiconductor substrate wherein the unwanted films remaining on the peripheral portion and the beveled portion is removed under a condition that the insulating film and the polysilicon film have non-selectivity to the semiconductor substrate.

Therefore, at the time of invention, it would have been obvious for those skilled in the art, in view of Inaoka et al., to modify process of Inaoka et al. by selectively grinding and polishing the peripheral portion and the beveled portion as being claimed to remove unwanted polylisilicon and insulating films from said peripheral and beveled portions. By doing, contamination to the semiconductor device can be reduced or eliminated.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanhha Pham whose telephone number is (571) 272-1696. The examiner can normally be reached on Monday and Thursday 9:00AM - 9:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thanhha Pham

C. Chandhari

Chandra Chaudhari
Primary Examiner